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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,269	05/25/2001	Sasan Cyrusian	10808/27	5524

757 7590 11/20/2002

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EXAMINER
COX, CASSANDRA F

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,269	CYRUSIAN, SASAN	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *20-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,7,10,13-16 and 19* is/are rejected.

7)☒ Claim(s) *2-3, 5, 8-9, 11-12,17-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's arguments with respect to claims 1, 4, 6-7, and 13-14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1, 4, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Proebsting (U.S. Patent No. 6,154,064).

In reference to claim 1, Proebsting discloses in Figure 1 a circuit comprising: a first amplifier having a first (16) and second (17) transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (16) is connected to a drain of the second transistor (17) and a gate of the second transistor (17) is connected to a drain of the first transistor (16); and a second amplifier having a third (14) and fourth (15) transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (OUT1, OUT2), wherein a differential input voltage (IN1, IN2) is connected to gates of the second amplifier transistors, and a control input and power supply voltage (40 through transistor 28) is connected to

sources (based on the examiner's understanding of the figures and specification) of the first amplifier. The same applies to claim 4, wherein a control input and supply voltage (30) is connected to the sources of the second amplifier.

In reference to claim 6, a positive supply voltage (30) is connected to the second amplifier and a negative supply voltage is connected to the first amplifier (40 through transistor MP8).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 10, 13-16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (U.S. Patent No. 6,215,364) in view of Proebsting (U.S. Patent No. 6,154,064).

In reference to claim 7 Hwang discloses in Figure 1 a voltage controlled oscillator comprising a first delay unit (28-1) and a second delay unit (28-2) wherein output terminals (Vout1, Vout2) of the first delay unit (28-1) are connected to gates (Vin1, Vin2) of the second amplifier of the second delay unit (28-2) of the second delay unit (assuming that there are only two delay units in the oscillator), and output terminals (Vout1, Vout2) of the second delay unit (28-1) are connected to gates (Vin1, Vin2) of the second amplifier of the first delay unit (28-1). Hwang does not disclose that the delay units have the specific connections as claimed. Proebsting discloses in Figure 1 a delay unit having a first amplifier having a first (16) and second (17) transistor

connected as a two-transistor positive amplifier, wherein a gate of the first transistor (16) is connected to a drain of the second transistor (17) and a gate of the second transistor (17) is connected to a drain of the first transistor (16); and a second amplifier having a third (14) and fourth (15) transistor, wherein a drain of the third and fourth transistors is connected to a drain of the first and second transistors to form output terminals (OUT1, OUT2) and wherein a control input and power supply voltage (40 through transistor 28) is connected to sources of the first amplifier. Therefore, it would have been obvious to one skilled in the art at the time of the invention that the circuit of Proebsting could be used in the oscillator circuit of Hwang as an alternative method of implementing the delay units using fewer transistors for the advantage of saving space and lowering costs. The same applies to claims 13 and 15.

In reference to claim 10, the circuit of Hwang discloses an additional delay unit (28-3, 28-4). The same applies to claim 14, 16, and 19 wherein output terminals (Vout1, Vout2) of a delay unit (28-1-28-3) are connected to gates (Vin1, Vin2) of a next delay unit, and output terminals of a last delay unit (28-4) are connected to the gates of the first delay unit (28-1).

Response to Arguments

5. Applicant's arguments filed 08/27/02 with respect to the restriction requirement have been fully considered but they are not persuasive. The combination does not require the specific connections of the delay units as called for in the subcombination. Therefore, the restriction requirement will not be withdrawn.

Double Patenting

6. Applicant is advised that should claim 13 be found allowable, claim 15 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

7. Claims 2-3, 5, 8-9, 11-12, and 17-18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claims 2, 8, 11-12, and 17 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3A wherein the first amplifier transistors (56, 58) are PMOS transistors and the second amplifier transistors (60, 62) are NMOS transistors in combination with the rest of the limitations of the base claims and any intervening claims. Claims 3 and 9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3A a positive supply voltage (Vpos) is connected to the first amplifier (56, 58) and a negative supply voltage (Vneg) is connected to the second amplifier (60, 62) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 5 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4A wherein the first amplifier transistors (76, 78) are NMOS transistors and the second

amplifier transistors (72, 74) are PMOS transistors in combination with the rest of the limitations of the base claims and any intervening claims. Claim 18 would be allowable because the closest prior art of record fails to show a circuit as shown in Figure 9 wherein a buffered output voltage (the output of buffer 109) of the charge pump (98) is a supply voltage to the first amplifiers (82, 84) in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Kenneth B. Wells
Primary Examiner

CC

November 18, 2002